

MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)(Affiliated to JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY HYDERABAD)
Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad**II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019**Subject: Principles of Electrical Engineering

Branch: ECE

Time: 3 hours

Max. Marks: 75

PART – A**I.** Answer **ALL** questions of the following**5x1Mark=5 Marks**

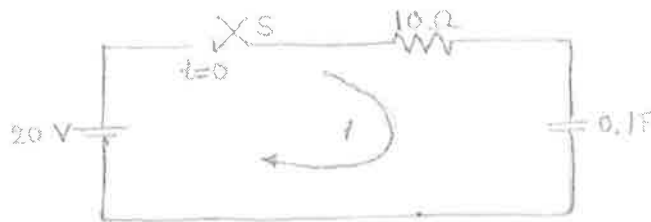
1. Write the expressions for time constant of an R-L circuit and R-C circuit.
2. Write the ABCD parameters?
3. Define Attenuator?
4. Draw the connection diagram of DC Shunt Motor?
5. Define mutual induction?

II. Answer **ALL** questions of the following**10x2Marks=20 Marks**

1. What is the difference between steady state and transient response
2. Draw the under damped response in series RLC circuit?
3. Define symmetrical property in two port networks and write the same for h and y parameters.
4. Write the Symmetry and Reciprocity conditions in h-parameters?
5. What is Symmetrical Attenuator
6. Write the applications of filters?
7. What is the principle of DC Motor?
8. Write the difference between short-shunt and long-shunt compound motors?
9. Write any two properties of Ideal Transformer?
10. Write the components of core loss in a transformer?

PART-BAnswer **ALL** questions of the following**5x10 Marks= 50Marks**

1. A series RC circuit consists of resistor of $10\ \Omega$ and capacitor of 0.1F as shown in Figure. A constant voltage of 20V is applied to the circuit at $t=0$. Obtain the current equation. Determine the voltages across the resistor and the capacitor.

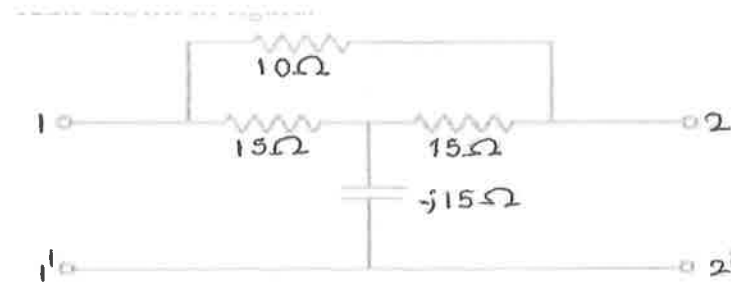
**(OR)**

2. a) A dc voltage of 20V is applied in a RL circuit where $R=5\Omega$ and $L=10\text{H}$. Find (i) the time constant
(ii) Current $i(t)$? (6M)
b) Explain the procedure to evaluate initial conditions? (4M)

3. Derive the condition for the symmetrical property in two port networks in case of admittance parameters.

(OR)

4. Determine the transmission parameters and hence determine the short circuit admittance parameters for the circuit shown in figure.



5. a) Explain the following to study and design a filter (i) Characteristic Impedance (ii) Propagation Constant (iii) Phase constant (iv) Attenuation constant (6M)
b) Describe the frequency response characteristics of low pass and high pass filter? (4M)

(OR)

6. a) What is a constant - K low pass filter, derive its characteristics impedance.
b) Design a band elimination filter having a design impedance of 600Ω and cut-off frequencies $f_1=2$ kHz and $f_2=6$ kHz.
7. a) Explain the torque-speed characteristics of a dc shunt, series motors.
b) Explain speed control methods of a DC shunt motor?

(OR)

8. a) Explain the classification of DC.Motors?
b) Explain the procedure to conduct Swinburne's test for predicting motor efficiency?
9. a) Derive the emf equation of a single-phase transformer?
b) Explain various losses in a transformer?

(OR)

10. a) Open circuit and short circuit tests conducted on a 10KVA, 500/2000V, 50 Hz, Single phase Transformer gave the following readings:
OC Test: 500V, 120W on LV side.
SC Test: 15V, 20A, 100W on HV side.
Determine the efficiency on full load at u.p.f
b) What is an ideal transformer? Explain.

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Gundlapochampally (H), Maisammaguda (V), Medchal (M), Medchal-Malkajiri (Dist), Hyderabad**II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019**Subject: Pulse and Digital Circuits

Branch: ECE

Time: 3 hours

Max. Marks: 75

PART – A**I.** Answer **ALL** questions of the following**5x1Mark=5 Marks**

1. What are the applications of Schmitt trigger?
2. Define transmission error?
3. Write the conditions of RC circuit of work as differentiator.
4. Define fan out?
5. List any two merits of cmos technology

II. Answer **ALL** questions of the following**10x2Marks=20 Marks**

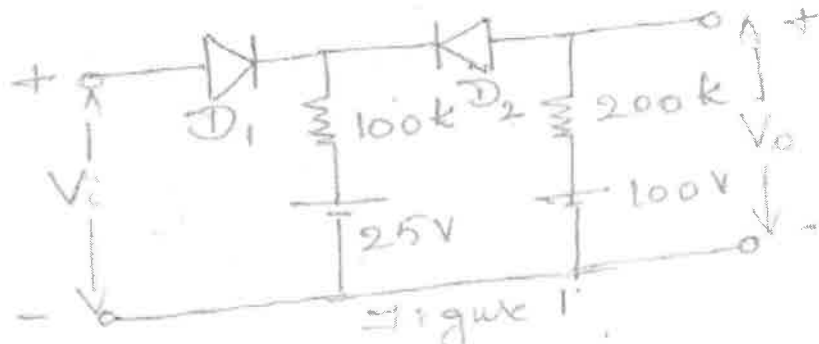
1. What are the methods to achieve linear sweep voltage wave form.
2. Write the application of sampling gates?
3. What is the synchronization?
4. Write a short notes on ECL.
5. Define displacement error?
6. Why is sampling referred as a linear gate?
7. Differentiate astable and monostable multi vibrators.
8. Write an expression for UTP and LTP of a schmitt trigger?
9. What are the advantages and disadvantages of uni directional diode gate.
10. Write short note on delay time?

PART-BAnswer **ALL** questions of the following**5x10 Marks= 50Marks**

1. a) A 10HZ symmetrical square wave whose peak to peak amplitude is 2V is impressed on a high pass circuit whose lower 3db frequency is 5Hz. calculate and sketch the peak output amplitude.
b) What is the peak to peak output amplitude of the above wave form?

OR

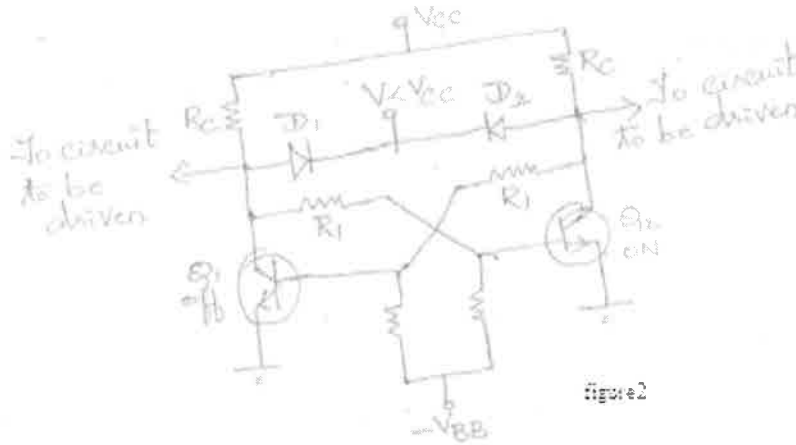
2. For the circuit shown in figure 1 an input voltage V_1 linearly varies from 0 to 150V is applied. Sketch the output voltage V_0 and transfer characteristics assume ideal diodes.



3. Draw the circuit of an emitter coupled clipping circuit. Explain its operation its transfer characteristics and necessary expressions.

OR

4. For the circuit shown in fig2, $V_{cc}=18V$, $V_{bb}=6V$, $V=6V$, $R_c=1.5K$, $R_1=5K$, $R_2=25K$ & $h_{FE}(\min)$ of each transistor is 40. Neglect the drop across the forward biased junctions. Indicate all the circuit voltage in the quiescent state and indicate also the voltage immediately after a 5V positive step is applied?



5. Describe the operation of a transistor voltage sweep wave form generator, employing a constant current charging method. What the help of its circuit diagram and waveforms?

OR

6. Discuss about triggering of monostable multi-vibrators. Does a monostable multivibrator need symmetrical triggering. Explain.
7. Explain the operation of bidirectional sampling gate using diodes. Give the equivalent circuit and derive the expression for gain. Derive the expression for minimum control voltages required?

OR

8. a) Explain the method of synchronization of a sinusoidal oscillator with pulses.
b) Explain the synchronization of a sweep circuit with symmetrical signals
9. Explain the working of a two diode sampling gate. Derive the expressions for
i) Gain ii) $(V_c)_{\min}$ iii) $(V_n)_{\min}$

OR

10. a) Explain TTL logic gate.
b) Compare RTL, DTL, DCTL, TTL, CMOS logic families.

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GundlapochampALLy (H), Maisammaguda (V), Medchal (M), Medchal-Malkajgiri (Dist), Hyderabad**II B.TECH II SEMESTER SUPPLEMENTARY EXAMINATIONS, MAY-2019**Subject: Digital Design Using Verilog HDL

Branch: ECE

Time: 3 hours

Max. Marks: 75

PART – A**I.** Answer **ALL** questions of the following**5x1Mark=5 Marks**

1. What are identifiers?
2. Write one Assignment statement with Delay in verilog.
3. Explain the significance of "casex" keyword.
4. Write the usage of \$period in verilog HDL.
5. Give example of the functional register.

II. Answer **ALL** questions of the following**10x2Marks=20 Marks**

1. How do you write comments in Verilog?
2. What are the categories of Data - types
3. Draw a R-S flip flop using NAND gates.
4. Write the XOR gate test benches of verilog
5. What is the use of forever construct
6. Write about fork - join construct
7. When is Hierarchical access used?
8. Explain about the test bench.
9. What is Hold time?
10. Explain basic memory components

PART-BAnswer **ALL** questions of the following**5x10 Marks= 50Marks**

1. Classify and explain 'strengths & contention resolution' used in Verilog?

OR

2. a) Explain top-down design methodology with example.
b) Write verilog half adder programe.
3. Explain continuous assignments statements with examples.

OR

4. Write verilog code and test bench for 4 – to- 1 multiplexer using data flow modeling
5. Explain about concept of conditional statements and write verilog code for latch with positive gate

OR

6. a) Design clocked D Flip Flop with verilog module
b) Design test bench of D Flip-Flop using assignment delay
7. Write a verilog program for 4-bit parallel adder using tasks and functions.

OR

8. a) Design CMOS RAM cell.

(b) Write verilog module programme for CMOS RAM cel

9. Explain the Implicit Model for Sequential circuits with examples

OR

10. Explain in detail about basic memory elements

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Branch: ECE

Time: 3 hours

Max. Marks: 75

PART – A

I. Answer ALL questions of the following

5x1Mark=5 Marks

1. Draw the circuit diagram of CB amplifier
2. What is the necessity of multistage amplifier?
3. Classify different types of oscillator.
4. What is push pull amplifier?
5. At what frequencies are the tuned amplifiers operate?

II. Answer ALL questions of the following

10x2Marks=20 Marks

1. Draw simplified CE hybrid model circuit.
2. Analyze general transistor amplifier circuit using h-parameter model.
3. Define miller theorem.
4. Draw Hybrid —pi (π) common emitter transistor model.
5. State the Barkhausen criterion for sustained oscillation. What will happen to the oscillations if the magnitude of the loop gain is greater than unity?
6. What are the conditions for oscillator?
7. What is the purpose of heat sink in power amplifiers?
8. Define conversion efficiency
9. What is the effect of cascading n stages of identical single tuned amplifiers on overall bandwidth?
10. What is the expression for resonant frequency?

PART-B

Answer ALL questions of the following

5x10 Marks= 50Marks

1. a) Derive input resistance, output resistance of transistor amplifier in CB configuration using h-parameters?
- b) Given a single stage transistor amplifier with h- parameters as $h_{ic} = 1.1 \text{ k}\Omega$, $h_{rc} = 1$, $h_{fc} = -51$, $h_{oc} = 25 \mu\text{A/V}$. Calculate A_i , A_v , A_{vs} , for the Common collector Configuration, with $R_s = R_L = 10\text{K}$.

OR

2. a) Draw the circuit diagram of CS amplifier and its small-signal equivalent circuit. Derive the expression for voltage gain and the output impedance.
- b) For CS amplifier with $R_D = 4\text{k}\Omega$, $r_d = 4\Omega$ and trans conductance of 0.8mA/V . Evaluate its voltage gain.
3. a) Derive CE short circuit current gain
- b) Explain in detail about hybrid - Π capacitances

OR

4. Compare emitter follower and Darlington emitter follower configurations in request of
 - a) Current gain
 - b) Input impedance
 - c) Voltage gain
 - d) Output impedance.

5. a) Explain in detail about effect of negative feedback?

b) For a series shunt feedback amplifier $A=100$, $\beta = 0.1$, $R_i = 1\text{ k}\Omega$, $R_o=50\Omega$, estimate R_{if} , R_{of} , A_f ?

OR

6. a) With neat diagram, explain the concept of feedback. Also explain each block used in feedback concept.

b) A negative feedback amplifier has $A=150$, $\beta = 0.04$ & $V_s=50\text{mV}$. Find (i) Gain with feedback (A_f) (ii) Output Voltage (V_o) (iii) Loop gain

7. a) Discuss about conversion efficiency of class B amplifier and derive the necessity equation.

b) Explain about two types of heat sinks?

OR

8. a) Write a short note on the requirement and types of heat sinks for power dissipation in large-signal amplifiers.

b) Calculate the total harmonic distortion for amplifier components given $D_2=0.1$, $D_3=0.05$, $D_4=0.01$

9. Draw and explain the circuit diagram of Double tuned capacitance amplifier. Also explain its operation

OR

10. What is tuned amplifier? Write about the classification of tuned amplifiers.